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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,223	02/27/2004	Fumitoshi Yamamoto	67161-142	4831

7590 03/28/2005

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,223	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *4-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7 February 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

2. The examiner notes that the applicant states (on p. 6 of the response filed on January 5, 2005) that claim 1 recites that the first cathode region and the second cathode region are separate regions. However claim 1 only states that the first cathode region is formed at a main surface of the substrate. The exact location of the second cathode region or its spatial relationship relative to the first cathode region is not described in the claim.

Specification

3. The examiner notes the newly amended title and thus hereby withdraws the objection made to the specification in the previous Office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Li et al. (USPN 6,268,639 B1).

6. In reference to claim 1, Li et al. (USPN 6,268,639 B1, hereinafter referred to as the "Li" reference) discloses a similar device. Figures 4A-4B of Li disclose a semiconductor device with a surge protection circuit that is electrically connected to a signal input terminal (V_A) and has a diode (405) and a transistor (415). The device has a semiconductor substrate (422) with a main surface. A field oxide (425 or 425') is formed at the main surface of the semiconductor substrate (422). A first conductive layer (silicide region 430 over 440 or the wiring denoted by the black line which leads to V_A; either of these two may be interpreted to be the conductive layer) is formed on the main surface of the semiconductor substrate (422) and is electrically connected to the signal input terminal (V_A). The diode has a cathode which includes a first cathode region (440) and a second cathode region (465). The first cathode region (440) is formed at the main surface of the substrate (422). The first cathode region (440) and the second cathode region (465) together with an anode region (460) of the diode form a pn junction where Zener breakdown occurs.

7. With regard to claim 2, the cathode (440) and a collector of the transistor are electrically connected to the signal input terminal (V_A). The anode (450) and the base are formed to be of the same conductivity type and are electrically connected to each other.

8. In reference to claim 3, the second cathode region (465) is formed to cover an upper surface of the anode region (450).

Allowable Subject Matter

9. Claims 4-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a semiconductor device having a surge protection circuit with a Zener diode and a bipolar transistor such that the Zener diode has a cathode region connected to a terminal and additional cathode regions in a semiconductor substrate such that the collector of the transistor includes an additional layer within the substrate and a buried layer within this additional layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

NATHAN J. FLYNN
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